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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/046,772	01/17/2002	Young-Ki Kim	6192.0249.AA	2680

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EXAMINER	
NGUYEN, JENNIFER T	
ART UNIT	PAPER NUMBER
2674	

DATE MAILED: 06/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/046,772	KIM, YOUNG-KI	
	Examiner	Art Unit	
	Jennifer T. Nguyen	2674	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 January 2002*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6-8 and 11-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *8,11 and 12* is/are allowed.

6)☒ Claim(s) *1-4,6,7,13-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office action is responsive to amendment filed on 03/28/2005.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-4, 6, 7, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jeong et al. (U.S. Patent No. 6,271,816) in view of Ozawa (Patent No.: 6,670,953).

Regarding claims 1 and 14, referring to Figs. 1A, 2C, and 2G, Jeong teaches a liquid crystal display, comprising: a liquid crystal panel including a plurality of gate lines (R0, R1), a plurality of insulated data lines (C0, C1) crossing the gate lines (R0, R1), and a plurality of first thin film transistors (106) each having a gate electrode connected to a gate line (R0) and a source electrode connected to a data line (C0), and a drain electrode connected to a liquid crystal capacitor; a gate driver (102) for sequentially supplying a gate-on voltage to the gate lines (R0, R1) for turning on the thin film transistors (106); a data driver (104) for applying a data voltage to the data lines (C0, C1); a data line sharing switch having a plurality of switching devices (112), each of which formed between the adjacent data lines (C0, C1); and a sharing signal generator for outputting a sharing control signal (i.e., neutralizer enable) for turning on the switching devices (112) to connect the adjacent data lines (col. 1. lines 10-67, col. 5, lines 1-67, and col. 6, lines 1-31).

Jeong differs from claims 1 and 14 in that he does not specifically teach the first thin film transistors are disposed between the data line sharing switch and the data driver. However, referring to Fig. 1, Ozawa teaches first thin film transistors are disposed between the data line sharing switch (T7a-T7c) and the data driver (i.e., a data driver includes a shift register 7) (col. 7, lines 16-34). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the thin film transistors are disposed between the data line sharing switch and the data driver as taught by Ozawa in the system of Jeong in order to avoid the density of elements at one end of the matrix display.

Regarding claim 2, Jeong further teaches the data line sharing switch is formed on the liquid crystal panel (col. 1, lines 16-67 and col. 6, lines 24-31).

Regarding claim 3, Jeong also teaches that the switching devices (112) are second thin film transistors (col. 5, lines 35-36).

Regarding claim 4, Jeong further teaches the second thin film transistors (112) are manufactured by the same process as the first thin film transistor (106) (Fig. 1A, col. 5, lines 1-67, col. 6, lines 1-31).

Regarding claim 6, Jeong further teaches the sharing signal generator applies a sharing signal pulse (i.e., neutralizer enable) for sharing the data lines (C0, C1) between the gate-on voltages applied to adjacent gate lines respectively (col. 5, lines 1-67, col. 6, lines 1-31).

Regarding claim 7, Jeong teaches the sharing signal generator applies a sharing signal pulse for sharing the data lines (C0, C1) after the voltage applied to the previous gate line turns to a gate-off voltage (col. 5, lines 1-67, col. 6, lines 1-31).

4. Claims 15-18 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Negishi et al. (Patent No.: 5,907,314) in view of Wright (EP 0 315 365).

Regarding claims 15-18 and 20, referring to Fig. 4, teaches a liquid crystal display (1), comprising: a liquid crystal panel including a plurality of gate lines (X1-Xn), a plurality of first and second data lines (Y1-Yn and (Y11-Ynn), and a plurality of first and second thin film transistors (5a) each having a gate electrode connected to a gate line (i.e., X1), a source electrode connected to a data line (i.e., Y1), and a drain electrode connected to a liquid crystal capacitor (5b); a gate driver (10) for sequentially supplying a gate-on voltage to the gate lines for turning on the first and the second thin film transistors; a first data driver (12) for applying a first data voltage to the first data lines; a second data driver (13) for applying a second data voltage to the second data lines (col. 11, line 8 to col. 12, line 33).

Negishi differs from claims 15-18 and 20 in that he does not specifically teach a first data sharing switch having a plurality for first switching devices, each of which formed between the adjacent first data lines; a second data line sharing switch having a plurality of second switching devices, each of which formed between the adjacent second data lines; and a sharing signal generator for outputting a first sharing control signal for turning on the first switching devices to connect the adjacent first data lines and a second sharing control signal for turning on the second switching devices to connect the adjacent second data lines, wherein the first thin film transistors are disposed between the first data line sharing switch and the first data driver, and the second thin film transistors are disposed between the second data line sharing switch and the second data driver. However, referring to Fig. 1, Wright teaches a first data sharing switch having a plurality for first switching devices (17-19), each of which formed between the adjacent first data lines

(2a-4a); a second data line sharing switch having a plurality of second switching devices (20-22), each of which formed between the adjacent second data lines (2c-4c); and a sharing signal generator (not shown) for outputting a first sharing control signal for turning on the first switching devices (17-19) to connect the adjacent first data lines and a second sharing control signal for turning on the second switching devices (20-22) to connect the adjacent second data lines (col. 2, line 48 to col. 3, line 35). Although Wright does not specifically teaches the first thin film transistors are disposed between the first data line sharing switch and the first data driver, and the second thin film transistors are disposed between the second data line sharing switch and the second data driver. Wright teaches first data line sharing switch and the second data line sharing switch disposed between two sub panels (Fig. 1) and Negishi teaches the upper driver circuit and lower driver circuit of two sub panels (Fig. 4). Therefore, it would have been obvious to obtain the first thin film transistors are disposed between the first data line sharing switch and the first data driver, and the second thin film transistors are disposed between the second data line sharing switch and the second data driver in order to drive the display panel more efficiently. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the first data line sharing switch and the second data line sharing switch as taught by Wright in the system of Negishi in order to provide an LCD for charging each data line for the LCD to sufficient voltage level, resulting high quality image display.

5. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jeong et al. (U.S. Patent No. 6,271,816) in view of Ozawa (Patent No.: 6,670,953) and further in view of Johnson et al. (Patent No.: US 6,304,254).

Regarding claim 13, the combination of Jeong and Ozawa differs from claim 13 in that it does not specifically teach the first and second thin film transistors comprise amorphous transistor. However, referring to Fig. 1, Johnson teaches the thin film transistors (3) comprise amorphous transistor (col. 3, lines 38-41). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the thin film transistors comprise amorphous transistor as taught by Johnson in the system of the combination of Jeong and Ozawa in order to provide a semiconductor layer with simple fabrication processes and high driving capacity.

6. Claims 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Negishi et al. (Patent No.: 5,907,314) in view of Wright (EP 0 315 365) and further in view of Johnson et al. (Patent No.: US 6,304,254).

Regarding claim 19, the combination of Negishi and Wright differs from claim 13 in that it does not specifically teach the first and second thin film transistors comprise amorphous transistor. However, referring to Fig. 1, Johnson teaches the thin film transistors (3) comprise amorphous transistor (col. 3, lines 38-41). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the thin film transistors comprise amorphous transistor as taught by Johnson in the system of the combination of Negishi and Wright in order to provide a semiconductor layer with simple fabrication processes and high driving capacity.

7. Claims 8 and 11-12 are allowed.

Response to Arguments

8. Applicants' arguments filed 03/28/2005, have been fully considered but they are not persuasive because as follows:

In response to Applicants' argument filed "the Office action has failed to provide any objective motivation in the prior art for combination these references, the combination is improper and fails to establish a *prima facie* case of obviousness of claims 1-4, 6, 7 and 14. Further Johnson fails to remedy any of these deficiencies". Examiner respectfully disagrees, Jeong and Ozawa both disclose an active matrix display with TFT switching unit, gate driver, data driver, and data line sharing switch (112, Fig. 1 of Jeong) and (T7a, Fig. 1 of Ozawa). Jeong teaches all claimed limitations (claims 1-4, 6, 7, and 14) except the first TFTs are disposed between the data line sharing switch and the data driver. Jeong teaches the data line sharing switch is disposed between first TFTs and the data driver (Fig. 1 of Jeong). However, Ozawa teaches the first TFTs (TFT of the pixels) are disposed between the data line sharing switch (T7a-T7c) and the data driver (7) (Fig. 1 of Ozawa). This is not adding the switches of Ozawa to the circuit of Jeong but shifting location of part to different position, which is not changing the function of the device. Therefore, the combination is proper. The Applicants' argument filed "a first data line sharing switch having a plurality of first switching devices, each of which formed between the adjacent first data lines...a second data line sharing switch having a plurality of second switching devices, each of switch formed between the adjacent second data lines. Neither Negishi nor Wright, either alone or in combination, discloses these elements". However, Wright teaches a first data line sharing switch having a plurality of first switching devices (17-19) and a second data line sharing switch having a plurality of second switching devices (20-22) disposed

between upper sub-panel and lower sub-panel (Fig. 1 of Wright). Negishi teaches an upper sub-panel (101) driving by an upper driver (112) and a lower sub-panel (102) driving by an lower driver (113), and it is well known in the art to have two data drivers to drive top and bottom panel in the matrix display. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the upper sub-panel driving by an upper driver and a lower sub-panel driving by an lower driver as taught by Negishi in the system of Wright in order to scan the lines more efficiently. Therefore, it is believed that the ground of the rejection is maintained.

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer T. Nguyen whose telephone number is 571-272-7696. The examiner can normally be reached on Mon-Fri: 9:00am-5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Patrick N. Edouard can be reached on 571-272-7603. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jennifer Nguyen
06/20/05

REGINA LIANG
PRIMARY EXAMINER